AMENDMENTS TO THE CLAIMS

1-47. (Canceled)

48. (Currently Amended) A method of forming a memory circuit for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions over said substrate to form a multi-region planar thyristor having at least four regions; and

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode,;

~~connecting~~ said at least one polysilicon gate adapted for connection to a voltage source for producing latch-up in said multi-region planar thyristor~~; and~~

~~incorporating said multi-region planar thyristor in a memory device~~.

49. (Original) The method of claim 48 wherein said step of providing doped silicon regions further comprises forming a seven-region planar thyristor.

50. (Original) The method of claim 49 wherein said step of providing doped silicon regions further comprises forming a p-n-p-n-p-n-p planar thyristor.

51. (Currently Amended) The method of claim ~~50~~ 49 wherein said step of providing doped silicon regions further comprises forming an n-p-n-p-n-p-n planar thyristor.

52. (Original) The method of claim 49 wherein said step of providing doped silicon regions further comprises forming two memory cells.

53. (Currently Amended) The method of claim 52 further comprising connecting a central region of said seven-region planar thyristor to a shared row address line for said two memory cells.

54. (Original) The method of claim 48 wherein said step of providing doped silicon regions further comprises forming one memory cell.

55. (Currently Amended) A method of forming a memory device for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions over said substrate to form a multi-region planar thyristor having at least four regions; and

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode, said gate adapted to receive a voltage from a voltage source for producing latch-up in said multi-region planar thyristor, latch-up representing one of said at least two possible stable current states.; ~~and~~

~~incorporating said multi-region planar thyristor in a memory device.~~

56. (Previously Presented) The method of claim 55 wherein said step of providing doped silicon regions further comprises forming a seven-region planar thyristor.

57. (Previously Presented) The method of claim 56 wherein said step of providing doped silicon regions further comprises forming a p-n-p-n-p-n-p planar thyristor.

58. (Previously Presented) The method of claim 56 wherein said step of providing doped silicon regions further comprises forming an n-p-n-p-n-p-n planar thyristor.

59. (Previously Presented) The method of claim 56 wherein said step of providing doped silicon regions further comprises forming two memory cells.

60. (Currently Amended) The method of claim 59 further comprising connecting a central region of said seven-region planar thyristor to a shared row address line for said two memory cells.

61. (Previously Presented) The method of claim 55 wherein said step of providing doped silicon regions further comprises forming one memory cell.

62. (Currently Amended) A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising:

providing a semiconductor substrate;

providing doped silicon regions over the substrate to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode; and

connecting said at least one polysilicon gate to ~~a voltage source for producing latch-up in said multi-region planar thyristor through~~ a write row address line of a memory integrated circuit, said thyristor being adapted to ~~transition from a first one to a second one of said at least two possible current states~~ connect through said write row address line to a voltage source for producing latch-up in said multi-region planar thyristor.

63. (Currently Amended) A method of forming a memory integrated circuit comprising:

forming a plurality of thyristor structures over a substrate;

forming a plurality of gates disposed over respective single junctions of said

plurality of thyristor structures;

forming ~~a plurality of channels~~ isolation regions disposed between said thyristor structures, whereby said thyristor structures are disposed in spaced relation to one another; and

mutually coupling at least two gates of said plurality of gates to a write row address line of said memory integrated circuit.

64. (Currently Amended) A method of forming a ~~circuit~~ memory device for storing information as one of at least two possible stable current states as defined in claim ~~48~~ 55 wherein said ~~incorporating said multi-region planar thyristor in a memory device comprises coupling said at least one polysilicon gate to a write row address line of said memory device~~ thyristor is adapted to transition from a first one to a second of said at least two current states in response to a change in voltage received by said thyristor.

65. (Currently Amended) A method of forming a device for storing information as one of at least two possible stable current states as defined in claim 55 wherein said ~~incorporating said multi-region planar thyristor in a memory device comprises coupling said at least one polysilicon gate to a write row address line of said memory device~~ semiconductor substrate comprises a silicon-on-insulator structure.

66. (New) The method of claim 63 wherein said step of forming isolation regions comprises etching trenches and filling said trenches with an insulating material.

67. (New) The method of claim 66 wherein said insulating material comprises an oxide.